WHAT IS CLAIMED IS:

1. A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M1};

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M2};

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1};

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2} ; and

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier.

2. The memory of Claim 1, wherein the first reference current circuit is activated when any one of the read-select inputs of the first plurality of memory cells is

activated, and wherein the second reference current circuit is activated when any one of the read-select inputs of the second plurality of memory cells is activated.

3. The memory device of Claim 1 further comprising:

a plurality of first read word lines, each first read word line being coupled to the read-select input of a respective one of the first plurality of memory cells;

a plurality of second read word lines, each second read word line being coupled to the read-select input of a respective one of the second plurality of memory cells; and

a read control/decoder that is responsive to a set of address bits and that has a plurality of control outputs, each first read word line being coupled to a respective one of the control outputs, each second read word line being coupled to a respective one of the control outputs, the enable input of the first current reference cell being coupled to a respective one of the control outputs, and the enable input of the second current reference cell being coupled to a respective one of the control outputs, said read control/decoder generating an activation signal to the first reference current circuit when it generates an activation signal to any one of the first read word lines, and further generating an activation signal to the second reference current circuit when it generates an activation signal to any one of the second read word lines.

4. The memory of Claim 1, wherein the data states of the first and second plurality of memory cells are selectively sensed by said current sense amplifier during a read operation, and wherein the read-select input of only one of the memory cells is activated during the read operation.

5. The memory of Claim 1, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.25 \cdot I_{M1}$ and approximately $0.75 \cdot I_{M1}$.

6. The memory of Claim 5, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.25 \cdot I_{M2}$ and approximately $0.75 \cdot I_{M2}$.

7. The memory of Claim 1, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.25 \cdot I_{M2}$ and approximately $0.75 \cdot I_{M2}$.

8. The memory of Claim 1, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.3 \cdot I_{M1}$ and approximately $0.6 \cdot I_{M1}$.

9. The memory of Claim 1, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.35 \cdot I_{M1}$ and approximately $0.45 \cdot I_{M1}$.

10. The memory of Claim 9, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.35 \cdot I_{M2}$ and approximately $0.45 \cdot I_{M2}$.

11. The memory of Claim 1, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.35 \cdot I_{M2}$ and approximately $0.45 \cdot I_{M2}$.

12. The memory of Claim 1, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit is equal to or less than approximately $0.5 \cdot I_{M1}$.

13 The memory of Claim 1, wherein each of the magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 100 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

14. The memory of Claim 1, wherein each of magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 500 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

15. The memory of Claim 1, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein each memory cell of the second plurality of memory cells generates a current of substantially zero magnitude to represent the first data state and a current having a magnitude of substantially I_{M2} to represent the second data state.

16. The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.2 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length

permitted for the transistor in the integrated-circuit technology used to construct the memory device.

17. The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.5 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

18. The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $[1.9 - N_W/160] \cdot L_{MIN}$, where NW is the number of word lines which are spanned by one of the bit lines, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

19. The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has W/L ratio of channel width to channel length, and wherein the W/L ratio is less than approximately $3.4 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

20. The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has W/L ratio of channel width to channel length, and wherein the W/L ratio is less than approximately $1.7 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

21. A current sense amplifier to be powered by a supply voltage provided between a first supply line and a second supply line, the sense amplifier comprising:

a first sense input for receiving a current;

a second sense input for receiving a current;

a first impedance element coupled between the first sense input and a source of constant voltage;

a second impedance element coupled between the second sense input and the source of constant voltage;

a pair of cross-coupled transistors, each cross-coupled transistor having its source terminal coupled to a respective one of the sense inputs, and further having its drain terminal coupled to the gate terminal of the other cross-coupled transistor;

a pair of cascode transistors, each cascode transistor having its gate terminal coupled to an enabling signal, and further having its source terminal coupled to the drain terminal of a respective one of the cross-coupled transistors, said enabling signal having a first state where the cascode transistors are placed in first conductive states and a second state where the cascode transistors are placed in second conductive states, the second conductive state of each cascode transistor being substantially less than the first conductive state of the cascode transistor; and

a transistor coupled between the drain terminals of the cross-coupled transistors for electrically coupling drain terminals of the cross-coupled transistors when the enabling signal is in its first state.

22. The current sense amplifier of Claim 21 further comprising a transistor coupled between the first and second sense terminals for electrically coupling the sense terminals to one another when the enabling signal is in its first state.

23. The current sense amplifier of Claim 21, wherein the first impedance element maintains the voltage of the first sense input at the constant voltage value to within a tolerance value, and wherein the second impedance element maintains the voltage of the second sense input at the constant voltage value to within the tolerance value, the tolerance value being 25% of the magnitude of the supply voltage.

24. The current sense amplifier of Claim 21, wherein the first impedance element maintains the voltage of the first sense input at the constant voltage value to within a tolerance value, and wherein the second impedance element maintains the voltage of the second sense input at the constant voltage value to within the tolerance value, the tolerance value being 15% of the magnitude of the supply voltage.

25. The current sense amplifier of Claim 21, wherein the source of constant voltage comprises one of the first and second supply lines.

26. The current sense amplifier of Claim 21, further comprising a current-driven voltage latch coupled to the outputs of the differential current generating circuit, the voltage latch generating an output voltage in relation to the difference in currents at the outputs of the differential current generating circuit.

27. The current sense amplifier of Claim 26, wherein the current-driven voltage latch comprises a pair of cross-coupled transistors, each cross-coupled transistor having its source terminal coupled to a second source of constant voltage, having its drain terminal coupled to a respective output of the differential current generating circuit, and having its drain terminal further coupled to the gate terminal of the other cross-coupled transistor.

28. A current sense amplifier to be powered by a supply voltage provided between a first supply line and a second supply line, the sense amplifier comprising:

a first sense input for receiving a current;

a second sense input for receiving a current;

a first impedance element coupled between the first sense input and a first source of constant voltage;

a second impedance element coupled between the second sense input and the source of constant voltage;

a differential current generating circuit having two inputs coupled to respective ones of the first and second sense inputs and two outputs, the input impedances of the

outputs being greater than the input impedances of the inputs, the differential current generating circuit generating differential currents at its outputs as a function of the difference in currents presented at its inputs; and

a current-driven voltage latch coupled to the outputs of the differential current generating circuit, the voltage latch generating an output voltage in relation to the difference in currents at the outputs of the differential current generating circuit.

29. The current sense amplifier of Claim 28, wherein the current-driven voltage latch comprises a pair of cross-coupled transistors, each cross-coupled transistor having its source terminal coupled to a second source of constant voltage, having its drain terminal coupled to a respective output of the differential current generating circuit, and having its drain terminal further coupled to the gate terminal of the other cross-coupled transistor.

30. The current sense amplifier of Claim 29, wherein the first source of constant voltage comprises one of the first and second supply lines, and wherein the second source of constant voltage comprises the other of the first and second supply lines.

31. The current sense amplifier of Claim 29, further comprising a first reset transistor having its source and drain terminals coupled to the source and drain terminals of one of the cross-coupled transistors and a second reset transistor having its source and drain terminals coupled to the source and drain terminals of the other of the cross-coupled transistors, the reset transistors resetting the voltages between the drain and source terminals of the cross-coupled transistors in response to a signal applied to gate terminals of the reset transistors.

32. The current sense amplifier of Claim 29, further comprising an equalizing transistor coupled between the drain terminals of the cross-coupled transistors, the equalizing transistor equalizing the voltages of the drain terminals of the cross-coupled transistor in response to a signal applied to the gate terminal of the equalizing transistor.

33. The current sense amplifier of Claim 28, wherein the first impedance element maintains the voltage of the first sense input at the constant voltage value to within a tolerance value, and wherein the second impedance element maintains the voltage of the second sense input at the constant voltage value to within the tolerance value, the tolerance value being 25% of the magnitude of the supply voltage.

34. The current sense amplifier of Claim 28, wherein the first impedance element maintains the voltage of the first sense input at the constant voltage value to within a tolerance value, and wherein the second impedance element maintains the voltage of the second sense input at the constant voltage value to within the tolerance value, the tolerance value being 15% of the magnitude of the supply voltage.

35. The current sense amplifier of Claim 28, wherein the differential current generating circuit is responsive to an enable signal in generating the currents at its outputs, the enable signal have an active state wherein the differential current generating circuit is responsive and an inactive state when the differential current generating circuit is not responsive, and wherein the sense amplifier further comprising a transistor coupled between the first and second sense terminals for electrically coupling the sense terminals on one another when the enable signal is in inactive state.

36. A current sense amplifier to be powered by a supply voltage provided between a first supply line and a second supply line, the sense amplifier comprising:

a first sense input for receiving a current;

a second sense input for receiving a current;

an enable signal having an active state and an inactive state;

a first impedance element coupled between the first sense input and a source of constant voltage;

a second impedance element coupled between the second sense input and the source of constant voltage;

a differential current generating circuit having two inputs coupled to respective ones of the first and second sense inputs and two outputs, the input impedances of the

outputs being greater than the input impedances of the inputs, the differential current generating circuit generating differential currents at its outputs as a function of the difference in currents presented at its inputs, the differential current generating circuit being responsive the to enable signal and generating its differential currents when the enable signal is in its active state; and

a transistor coupled between the first and second sense terminals for electrically coupling the sense terminal when the enable signal is in its inactive state.

37. The current sense amplifier of Claim 36, wherein the source of constant voltage comprises one of the first and second supply lines.

38. A method of reading data stored in a memory, the memory having a first plurality of memory cells and a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, each memory cell of the first plurality of memory cells having its read output coupled to a first bit line and generating a current at its read output that has a magnitude less than or equal to a maximum magnitude I_{M1}, each memory cell of the second plurality of memory cells having its read output coupled to a second bit line and generating a current at its read output that has a magnitude less than or equal to a maximum magnitude I_{M2}, said method comprising the steps of:

(a) selecting a memory cell in one of the first and second plurality of memory cells by providing a signal to its read-select input;

(b) coupling a current I_{R1} to the second bit line when step (a) selects a memory cell of the first plurality of memory cells, the magnitude of current I_{R1} being less than or equal to $0.7 \cdot I_{M1}$;

(c) coupling a current I_{R2} to the first bit line when step (a) selects a memory cell of the second plurality of memory cells, the magnitude of current I_{R2} being less than or equal to $0.7 \cdot I_{M2}$; and

(d) sensing a difference in the currents on the first and second bit lines with a current sense amplifier.

39. The method of Claim 38, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} ranges between approximately $0.3 \cdot I_{M1}$ and approximately $0.6 \cdot I_{M1}$.

40. The method of Claim 39, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} ranges between approximately $0.3 \cdot I_{M2}$ and approximately $0.6 \cdot I_{M2}$.